

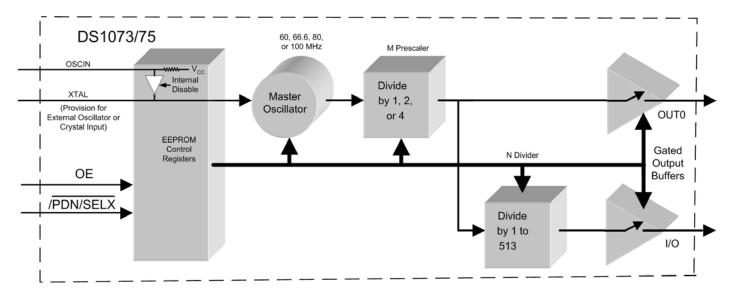
## Application Note 205 Configuring Standard DS1073 and DS1075 EconOscillators for Standalone Operation

#### www.maxim-ic.com

#### INTRODUCTION

The DS1073 and DS1075 EconOscillators<sup>TM</sup> each come in four standard options, with 60MHz, 66.666MHz, 80MHz, or 100MHz master oscillators as shown in Figure 1. In the standard parts, the M prescaler and the N divider, which may be set to numerous combinations of subfrequencies of the master oscillator, are set to 1 and 2, respectively. This provides an output at I/O of  $\frac{1}{2}$  the master frequency. In these standard parts, OUT0 is disabled, OE is configured to enable the oscillator output gate at I/O when tied to V<sub>CC</sub>, and /PDN/SEL is configured to shut down the oscillator altogether (putting it into a low-power mode) when tied to GND and enables the oscillator when tied to V<sub>CC</sub>. The inputs for the external clock or crystal inputs are disabled and only the internal oscillator is used to generate the clock output.

## DS1073 AND DS1075 BLOCK DIAGRAM Figure 1



EconOscillator is a trademark of Dallas Semiconductor.

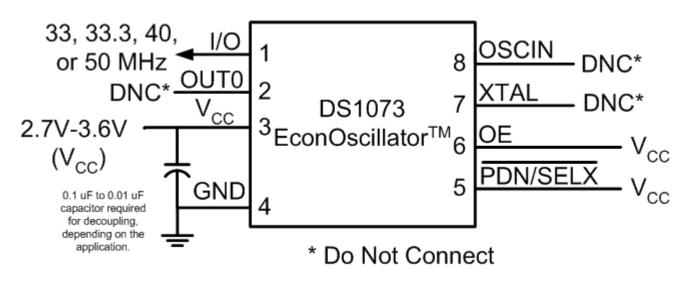
Table 1 shows the ordering options for both the DS1075 (5V) and the DS1073 (3.3V) EconOscillators.

IADLE I										
PART NO.	MASTER	I/O	OUT0	Μ	Ν	OE	PDN/SEL	I/O	V <sub>CC</sub>	PACKAGE
	FREQ							FREQ	<b>(V)</b>	
	(MHz)							(MHz)		
DS1073Z-60	60	EN	DIS	1	2	OE	PDN	30.000	5	8-SO
DS1073Z-66	66.6	EN	DIS	1	2	OE	PDN	33.333	5	8-SO
DS1073Z-80	80	EN	DIS	1	2	OE	PDN	40.000	5	8-SO
DS1073Z-100	100	EN	DIS	1	2	OE	PDN	50.000	5	8-SO
DS1075Z-60	60	EN	DIS	1	2	OE	PDN	30.000	3.3	8-SO
DS1075Z-66	66.6	EN	DIS	1	2	OE	PDN	33.333	3.3	8-SO
DS1075Z-80	80	EN	DIS	1	2	OE	PDN	40.000	3.3	8-SO
DS1075Z-100	100	EN	DIS	1	2	OE	PDN	50.000	3.3	8-SO

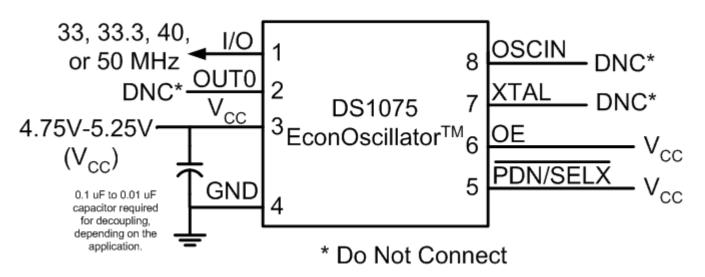
### **TABLE 1**

In standalone operation, typical configurations for the DS1073 (Figure 2) and DS1075 (Figure 3) are shown below. OSCIN and XTAL are internally disabled and OSCIN is internally tied high. Both of these inputs should be left open. Both control inputs, OE and /PDN/SEL should be tied to  $V_{CC}$  to enable the I/O output gate and enable the master oscillator, respectively. I/O will be the clock output,  $\frac{1}{2}$  the frequency of the master oscillator, and is able to drive 10 TTL/CMOS inputs. OUT0 is disabled and should be left disconnected.

# DS1073 CONFIGURATION Figure 2



# DS1075 CONFIGURATION Figure 3



Further information on the DS1073 can be found at: <u>http://dbserv.maxim-ic.com/quick\_view2.cfm?qv\_pk=2617</u>.

Further information on the DS1075 can be found at: <u>http://dbserv.maxim-ic.com/quick\_view2.cfm?qv\_pk=2619</u>.

These quickview data sheets also include links to an online interactive frequency calculator, which permits the calculation of other frequencies available from the DS1073 and DS1075.